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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/806,866	03/22/2004	Robert Tod Dimpsey	AUS920040065US1	2686

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ART UNIT	PAPER NUMBER
2185	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/806,866	DIMPSEY ET AL.	
	Examiner	Art Unit	
	Arpan P. Savla	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 June 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-8,12,15-18 and 21-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-8,12,15-18 and 21-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3/29/07, 6/29/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on June 29, 2007 has been entered.

Response to Amendment

This Office action is in response to Applicant's communication filed June 29, 2007 in response to the Office action dated March 29, 2007. Claims 1, 12, and 18 have been amended. Claims 2-3, 13-14, and 19-20 have been cancelled. New claim 24 has been added. Claims 1, 4-8, 12, 15-18, and 21-24 are pending in this application.

OBJECTIONS

Specification

1. In view of Applicant's amendments, the objection to the specification has been withdrawn.

Claims

2. **Claims 1, 6, 12, 17-18, and 23-24** are objected for the use of the term "one of...**or**..." The Examiner suggests Applicant amend to the term to instead read "one of...**and**..." as does appear in various limitations of claims 1, 12, 18, and 24. Appropriate correction required.

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 4-8, 12, 15-18, and 21-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Damron (U.S. Patent 6,782,454) in view of Hooker (U.S. Patent Application Publication 2003/0191900).

5. **As per claims 1 and 18**, Damron discloses a method in a data processing system for providing hardware assistance to prefetch data during execution of code by a processor in the data processing system, the method comprising:

responsive to loading of an instruction in the code into a cache, determining, by a processor unit, whether metadata for a prefetch is present for the instruction, wherein the metadata comprises a prefetch indicator that is associated with the instruction by one of being placed in the instruction or stored in a shadow memory (col. 4, lines 58-61;

col. 5, lines 17-24; Fig. 1, element 175; Fig. 3, element 220); *It should be noted that computer program product in claims 18-23 executes the exact same functions as the methods in claims 1 and 4-6. Therefore, any references that teach claims 1-6 also teach the corresponding claims 18 and 21-23. It should also be noted that the "prefetch request" is analogous to the "instruction", the "prefetch engine" is analogous to the "processing unit", and the "starting address of a node (to be prefetched), an offset value, and a termination value" all in combination are analogous to the "metadata." Lastly, it should be noted that the "starting address of a node (to be prefetched)" and the "offset value", which are placed in the prefetch request, are analogous to the "prefetch indicator" being placed in the instruction.*

responsive to determination of the metadata being present for the instruction, determining whether data is to be prefetched (col. 5, lines 27-35; Fig. 3, element 230); *It should be noted that "determining whether a termination condition has been satisfied" is analogous to "determining whether data is to be prefetched." Data is prefetched until the termination condition is met.*

and responsive to a determination that data is to be prefetched, prefetching data, from within a data structure using the metadata, into the cache in the processor (col. 5, lines 24-26 and 35-42; Fig. 3, elements 225 and 235). *It should be noted that responsive to the termination condition not being met, data is prefetched.*

Damron does not expressly disclose wherein the step of determining whether data is to be prefetched comprises one of determining whether a number of outstanding

cache misses is less than a threshold, and determining whether a number of cache lines chosen to be replaced is greater than a threshold;

and wherein the step of prefetching comprises one of prefetching the data responsive to determining that the number of outstanding cache misses is less than the threshold, and prefetching the data responsive to determining that the number of cache lines chosen to be replaced is greater than the threshold.

Hooker discloses wherein the step of determining whether data is to be prefetched comprises one of determining whether a number of outstanding cache misses is less than a threshold, and determining whether a number of cache lines chosen to be replaced is greater than a threshold (paragraph 0069; Fig. 5, element 536); *It should be noted that the "response buffers" are analogous to the "cache lines."*

and wherein the step of prefetching comprises one of prefetching the data responsive to determining that the number of outstanding cache misses is less than the threshold, and prefetching the data responsive to determining that the number of cache lines chosen to be replaced is greater than the threshold (paragraph 0070; Fig. 5, element 538).

Damron and Hooker are analogous art because they are from the same field of endeavor, that being prefetching memory systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Hooker's threshold based prefetch method within Damron's prefetch engine because, advantageously, by not prefetching cache lines if not enough free response buffers exist, the efficiency of a microprocessor is potentially increased.

Therefore, it would have been obvious to combine Damron and Hooker for the benefit of obtaining the invention as specified in claims 1 and 18.

6. **As per claims 4 and 21**, the combination of Damron/Hooker discloses retrieving the data from within the data structure using a pointer and an offset value (Damron, col. 5, lines 20-21). *It should be noted that the "starting address of a node" is analogous to a "pointer."*

7. **As per claims 5 and 22**, the combination of Damron/Hooker discloses retrieving the data from the data structure using an address (Damron, col. 5, lines 20-21).

8. **As per claims 6 and 23**, the combination of Damron/Hooker discloses the processor unit is selected from one of an instruction cache or a load/store unit (Damron, col. 4, lines 58-61; Fig. 1, element 175). *It should be noted that the "prefetch engine" is analogous to a "load/store unit."*

9. **As per claim 7**, the combination of Damron/Hooker discloses the cache is an instruction cache (Damron, col. 4, lines 53-54).

10. **As per claim 8**, the combination of Damron/Hooker discloses the metadata includes the pointer and the offset value (Damron, col. 5, lines 20-21). *See the citation note for claims 4 and 21 above.*

11. **As per claim 12**, Damron discloses a data processing system for providing hardware assistance to prefetch data during execution of code by a processor in the data processing system, the data processing system comprising:

first determining means, responsive to loading of an instruction in the code into a cache, for determining, by a processor unit, whether metadata for a prefetch is present

for the instruction, wherein the metadata comprises a prefetch indicator that is associated with the instruction by one of being placed in the instruction or stored in a shadow memory (col. 4, lines 58-61; col. 5, lines 17-24; Fig. 1, element 175; Fig. 3, element 220); *It should be noted that pg. 13, lines 3-5 of Applicant's specification appear to define this means as a computer. Also, see the citation note for the similar limitation in claims 1 and 18 above.*

second determining means, responsive to determination of the metadata being present for the instruction, for determining whether data is to be prefetched (col. 5, lines 27-35; Fig. 3, element 230); *It should be noted that pg. 13, lines 3-5 of Applicant's specification appear to define this means as a computer. Also, see the citation note for the similar limitation in claims 1 and 18 above.*

and prefetching means, responsive to a determination that data is to be prefetched, for prefetching data, from within a data structure using the metadata, into the cache in the processor (col. 5, lines 24-26 and 35-42; Fig. 3, elements 225 and 235). *It should be noted that pg. 13, lines 3-5 of Applicant's specification appear to define this means as a computer.*

Damron does not expressly disclose wherein the second determining means comprises one of means for determining whether data is to be prefetched comprises one of determining whether a number of outstanding cache misses is less than a threshold, and means for determining whether a number of cache lines chosen to be replaced is greater than a threshold;

and wherein the prefetching means comprises one of means for prefetching the data responsive to determining that the number of outstanding cache misses is less than the threshold, and means for prefetching the data responsive to determining that the number of cache lines chosen to be replaced is greater than the threshold.

Hooker discloses wherein the second determining means comprises one of means for determining whether data is to be prefetched comprises one of determining whether a number of outstanding cache misses is less than a threshold, and means for determining whether a number of cache lines chosen to be replaced is greater than a threshold (paragraph 0069; Fig. 5, element 536); *See the citation note for the similar limitation in claims 1 and 18 above.*

and wherein the prefetching means comprises one of means for prefetching the data responsive to determining that the number of outstanding cache misses is less than the threshold, and means for prefetching the data responsive to determining that the number of cache lines chosen to be replaced is greater than the threshold (paragraph 0070; Fig. 5, element 538).

Damron and Hooker are analogous art because they are from the same field of endeavor, that being prefetching memory systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Hooker's threshold based prefetch method within Damron's prefetch engine because, advantageously, by not prefetching cache lines if not enough free response buffers exist, the efficiency of a microprocessor is potentially increased.

Therefore, it would have been obvious to combine Damron and Hooker for the benefit of obtaining the invention as specified in claim 12.

12. **As per claim 15**, the combination of Damron/Hooker discloses retrieving means for retrieving the data from within the data structure using a pointer and an offset value (Damron, col. 5, lines 20-21). *It should be noted that pg. 13, lines 3-5 of Applicant's specification appear to define this means as a computer. Also, see the citation note for the similar limitation in claims 4 and 21 above.*

13. **As per claim 16**, the combination of Damron/Hooker discloses retrieving means for retrieving the data from the data structure using an address (Damron, col. 5, lines 20-21). *It should be noted that pg. 13, lines 3-5 of Applicant's specification appear to define this means as a computer.*

14. **As per claim 17**, the combination of Damron/Hooker discloses the processor unit is selected from one of an instruction cache or a load/store unit (Damron, col. 4, lines 58-61; Fig. 1, element 175). *It should be noted that pg. 13, lines 3-5 of Applicant's specification appear to define this means as a computer. Also, see the citation note for the similar limitation in claims 6 and 23 above.*

15. **As per claim 24**, Damron discloses a method in a data processing system for providing hardware assistance to prefetch data during execution of code by a processor in the data processing system, the method comprising:

responsive to loading of an instruction in the code into a cache, determining, by a processor unit, whether metadata for a prefetch is present for the instruction (col. 4, lines 58-61; col. 5, lines 17-24; Fig. 1, element 175; Fig. 3, element 220), wherein, the

processor unit comprises one of the instruction cache or a load/store unit (col. 4, lines 58-61; Fig. 1, element 175), and wherein the metadata comprises a prefetch indicator that is associated with the instruction by one of being placed in the instruction or stored in a shadow memory (col. 4, lines 58-61; col. 5, lines 17-24; Fig. 1, element 175; Fig. 3, element 220),and comprises a pointer and an offset value (col. 5, lines 20-21);

responsive to determination of the metadata being present for the instruction, determining whether data is to be prefetched (col. 5, lines 27-35; Fig. 3, element 230); *It should be noted that "determining whether a termination condition has been satisfied" is analogous to "determining whether data is to be prefetched." Data is prefetched until the termination condition is met.*

and responsive to a determination that data is to be prefetched, prefetching data, from within a data structure using the metadata, into the cache in the processor (col. 5, lines 24-26 and 35-42; Fig. 3, elements 225 and 235).

Damron does not expressly disclose wherein the step of determining whether data is to be prefetched comprises one of determining whether a number of outstanding cache misses is less than a threshold, and determining whether a number of cache lines chosen to be replaced is greater than a threshold;

and wherein the step of prefetching comprises one of prefetching the data responsive to determining that the number of outstanding cache misses is less than the threshold, and prefetching the data responsive to determining that the number of cache lines chosen to be replaced is greater than the threshold.

Hooker discloses wherein the step of determining whether data is to be prefetched comprises one of determining whether a number of outstanding cache misses is less than a threshold, and determining whether a number of cache lines chosen to be replaced is greater than a threshold (paragraph 0069; Fig. 5, element 536);

and wherein the step of prefetching comprises one of prefetching the data responsive to determining that the number of outstanding cache misses is less than the threshold, and prefetching the data responsive to determining that the number of cache lines chosen to be replaced is greater than the threshold (paragraph 0070; Fig. 5, element 538).

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Hooker's threshold based prefetch method within Damron's prefetch engine because, advantageously, by not prefetching cache lines if not enough free response buffers exist, the efficiency of a microprocessor is potentially increased.

Therefore, it would have been obvious to combine Damron and Hooker for the benefit of obtaining the invention as specified in claim 24.

Response to Arguments

16. Applicant's arguments filed June 29, 2007 with respect to claims **1, 4-8, 12, 15-18, and 21-23** have been fully considered but they are not persuasive.

17. With respect to Applicant's argument in the first full paragraph on page 8 of the communication filed June 29, 2007, the Examiner respectfully disagrees and directs

Applicant to the rejection of claims 1, 12, 18, and 24 above. As the Examiner pointed out above, not just the termination value alone, but rather the starting address of a node (to be prefetched), offset value, and termination value of Damron all in combination are analogous to Applicant's metadata. The starting address and offset value are supplied as part of the prefetch request in order to indicate the location of the first node to be prefetched. Thus, it is clear that Damron's "starting address of a node (to be prefetched)" and "offset value" are analogous to Applicant's "prefetch indicator" as simply and broadly claimed. It should also be noted that the starting address of a node, offset value, and termination value are all part of the prefetch request itself (i.e. the starting address of a node, offset value, and termination value are placed in the prefetch request). Accordingly, Damron sufficiently discloses the metadata comprises a prefetch indicator that is associated with the instruction by one of being placed in the instruction and stored in a shadow memory.

18. With respect to Applicant's argument in the second full paragraph on page 8 of the communication filed June 29, 2007, the Examiner respectfully disagrees and directs Applicant to the rejection of claims 1, 12, 18, and 24 above. The rationale behind the rejection is the Examiner has applied a known technique to a know device ready for improvement to yield predictable results. Thus, it would have been obvious to modify Damron in view of Hooker as indicated above because, advantageously, by not prefetching cache lines if not enough free response buffers exist, the efficiency of a microprocessor is potentially increased.

19. As for Applicant's arguments with respect to the dependent claims, the arguments rely on the allegation that independent claims 1, 12, and 18 are allowable and therefore for the same reasons the dependent claims are allowable. However, as addressed above, independent claims 1, 12, and 18 are not allowable, thus, Applicant's arguments with respect to the dependent claims are not persuasive.

Conclusion

STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by MPEP 707.70(i):

CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, **claims 1, 4-8, 12, 15-18, and 21-24** have received a first action on the merits and are subject of a first action non-final.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Arpan P. Savla whose telephone number is (571) 272-1077. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on (571) 272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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